UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,054	10/05/2000	Shinji Nakamura	0819-430	7323

7590 12/04/2002

Eric J. Robinson
Nixon Peabody LLP
8180 Greensboro Drive Suite 800
McLean, VA 22102

EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/680,054	NAKAMURA ET AL
	Examiner	Art Unit
	Brook Kebede	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *1-16 and 30-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-29 and 44-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed on November 4, 2002 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because PTO-1449 is missing. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 52-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 52 recites the limitation "wherein **n** is an arbitrary number other than 0" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claims 53-60 are rejected as being dependent of the rejected independent base claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 17-29 and 44-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuda et al. (US/6,335,546).

Re claims 17 and 18, Tsuda et al. disclose a method for the manufacture of a semiconductor device comprising: a step of preparing a substrate (i.e. sapphire substrate) (400) in which a surface (i.e. GaN) therefore is formed a depression (403) having triangle or hexagonal figure (see Fig. 9D) when viewed from the substrate normal; and a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, n) wherein said number n id an arbitrary number other than 0, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 19, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 20, as applied to claim 19 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression forming step includes step of forming on said major surface of said substrate defined by a (0, 0, 0, 1) plane a depression having a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 21, as applied to claim 17 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 22, as applied to claim 21 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 23, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 24, as applied to claim 23 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 25, as applied to claim 17 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 26, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 27, as applied to claim 25 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 28, as applied to claim 26 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 29, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said substrate preparing step is the step of preparing a sapphire substrate on which surface is formed a Group III nitride-based compound semiconductor layer; and wherein said depression forming step is the step of forming said depression in a surface of said Group III nitride-based compound semiconductor layer (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 44, Tsuda et al. disclose a method for the manufacture of a semiconductor substrate including: a step of preparing a substrate (400) for crystal growth; a step of depositing on said crystal growth substrate a first semiconductor layer (402) having a hexagonal crystal structure; a step of exposing either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane by subjecting a part of said first semiconductor layer to an etching process; and after said exposing step, a step of depositing on said first semiconductor layer a second semiconductor layer having a hexagonal crystal (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 45, as applied to claim 44 above, Tsuda et al. disclose all the limitations including a step of applying onto said first semiconductor layer a resist pattern having an opening whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and a step of forming a depression by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said depression has an inside face comprising either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 46, as applied to claim 45 above, Tsuda et al. disclose all the limitations including the limitation wherein said resist pattern has a plurality of said openings arrayed at equal intervals (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 47, as applied to claim 44 above, Tsuda et al. disclose all the limitations including a step of applying onto said first semiconductor layer a resist pattern whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed

from the substrate normal; and a step of forming a projection by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said projection has a side face comprising either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 48, as applied to claim 47 above, Tsuda et al. disclose all the limitations including the limitation wherein said resist pattern comprises a plurality of said resist patterns arrayed at equal intervals (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 49, Tsuda et al. disclose a method for the manufacture of a semiconductor substrate comprising: a step of forming a substrate (i.e. sapphire substrate) (400) in which a surface (i.e. GaN) therefore is formed a depression (403) having triangle or hexagonal figure (see Fig. 9D) when viewed from the substrate normal; a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure; and a step of taking out said semiconductor layer by removal of said substrate, wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, n) wherein said number n id an arbitrary number other than 0, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 50, as applied to claim 49 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression has an inside face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 51, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 52, Tsuda et al, disclose a method for the manufacture of a semiconductor substrate comprising: a step of forming a substrate having on a surface thereof a triangle or hexagonal projection; a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure; and a step of taking out said semiconductor layer by removal of said substrate, wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, n) wherein said number n id an arbitrary number other than 0, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 53, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said projection has a side face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 54, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said projection has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 55, as applied to claim 49 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of

forming a layer of Group III nitride-based compound semiconductor (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 56, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 57, as applied to claim 57 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 58, as applied to claim 56 above, Tsuda et al. disclose all the claimed limitations including the limitation, wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 59, as applied to claim 49 above, Tsuda et al. disclose all the claimed limitations including the limitation said substrate forming step including: a step of preparing a sapphire substrate; and a step of forming on said sapphire substrate a Group III nitride-based compound semiconductor layer having said depression in a surface thereof (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 60, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation said substrate forming step including: a step of preparing a sapphire substrate; and a step of forming on said sapphire substrate a Group III nitride-based

compound semiconductor layer having said projection on a surface thereof (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Response to Arguments

7. Applicant's arguments with respect to claims 17-29 and 44-60 have been considered but are moot in view of the new ground(s) of rejection that was by the amendment filed on September 9, 2002.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nidou et al. (JP/09199419) disclose method of growing a GaN (i.e., depression layer) on sapphire substrate having faces orientation (1, -1, 0, 1) on the surface. As Nidou et al. suggest, the crystal growth speed in the direction vertical to (1, -1, 0, 1) face is slow and the atomic migration of the above plane, i.e., (1, -1, 0, 1) is intensified. As result, a hexagonal gallium nitride compound semiconductor, which is smooth on the surface of in the direction parallel surface and having uniform C-axial orientation direction (i.e., the substrate normal) is formed. Hence, Nidou et al. also can be applied to reject the instant application claimed invention under 35 U.S.C. § 102.

9. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
November 29, 2002

SPE
Art Unit 2823